Supporting information: Gate defined confinement in bilayer graphene - hexagonal boron nitride hybrid devices

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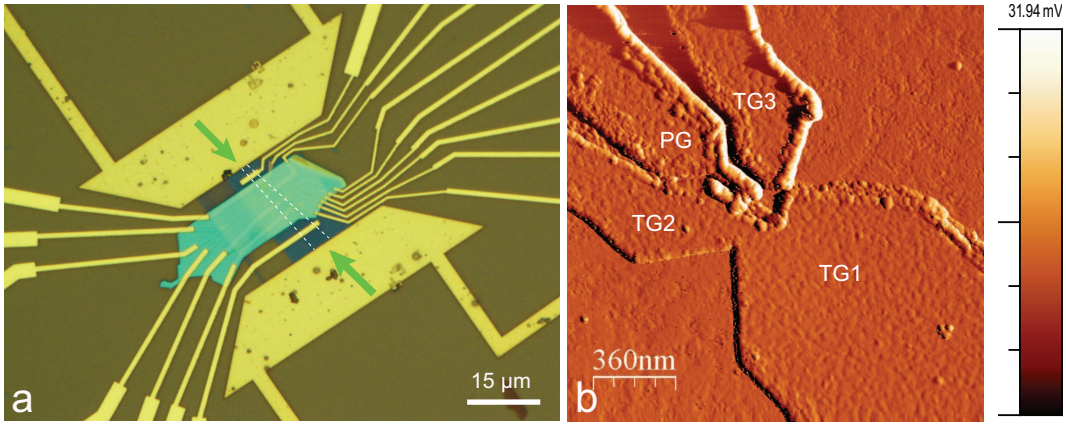

Figure 1: (a) Optical microscope image at 100x magnification. The green arrows indicate the location of the graphene. The top hBN dielectric is light blue, the bottom hBN dielectric below the graphene is dark blue. Contact and gate electrodes are yellow. The fine gate structures are hard to distinguish as they are only 15 nm thick. (b) AFM image of device B. It is clear from this image that TG1 and TG2 are electrically connected. PG and TG2 are not electrically connected.

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Background resistance subtraction procedure and alternatives for point contact conductance data

The main paper presents top gate traces for a constriction in device B after subtraction of a background resistance resulting in conductance plateaus at 6, 4 and 2 e^2/h. There are different scenarios possible for subtraction of a background series resistance and/or a parallel conductance, as outlined in footnote [22]. In figure 2 we show top gate traces for various scenarios for two typical datasets. On the left are the data for device A and on the right the data for device B (figure 2b in the main paper).

(a) Top gate traces (raw data) for device A at backgate voltages from -49.26 (leftmost) V to -49.74 V (rightmost) in 10 equal steps of -48 mV ($V_{bias} = 0.5$ mV, $T = 35$ mK and $V_{TG2} = 7$ V).

(b) Data of panel (a) after subtracting a background resistance (see inset) to to put the upper plateau at $6e^2/h$. Note that the background resistance is much lower than in fig. 2b of the main paper. This is because the graphene leads were damaged in between measuring device A and B.

(c) Data of panel (a) after subtracting a background resistance (see inset) to to put the upper plateau at $8e^2/h$.

(d) Data of panel (a) after first subtracting a parallel conductance (see inset) to put the conductance minimum at 0, and next subtracting a background resistance (see inset) in series with the device to put the upper plateau at $8e^2/h$

(e) Top gate traces for device B (raw data, same as figure 2b in the main paper) at back gate voltages from -49.26 V (leftmost) to -49.74 V (rightmost) in 10 equal steps of -48 mV ($V_{bias} = 0.5$ mV, $T = 35$ mK).

(f) Data of panel (e) after subtracting a background resistance (see inset) to to put the upper plateau at $6e^2/h$.

(g) Data of panel (e) after subtracting a background resistance (see inset) to to put the upper plateau at $8e^2/h$.

(h) Data of figure (e) after first subtracting a parallel conductance (see inset) to put the con-

ductance minimum at 0, and next subtracting a background resistance (see inset) in series with the device to put the upper plateau at 8 e^2/h.

All traces have been corrected for a known filter resistance of 5 kOhm and current amplifier input impedance of 2.1 kOhm. Also in the raw data of figure 2 these resistances are already subtracted since they are extrinsic to the device. The background resistance consists of a contact resistance, graphene lead resistance and Maxwell spreading resistance. From 4 terminal measurements at high density we can estimate that the contact resistance is in the order of 1 kOhm. The Maxwell spreading resistance is approximately $\pi^{-1}\rho \ln(W_{flake}/l)$ where ρ is the resistivity of the graphene, W_{flake} the width of the flake and l the mean free path. As the resistivity of the high mobility graphene around the point contact is relatively low, this term is in the order of a few hundred Ohms. The rest of the background resistance is made up of the graphene leads from the metal contact to the point contact.

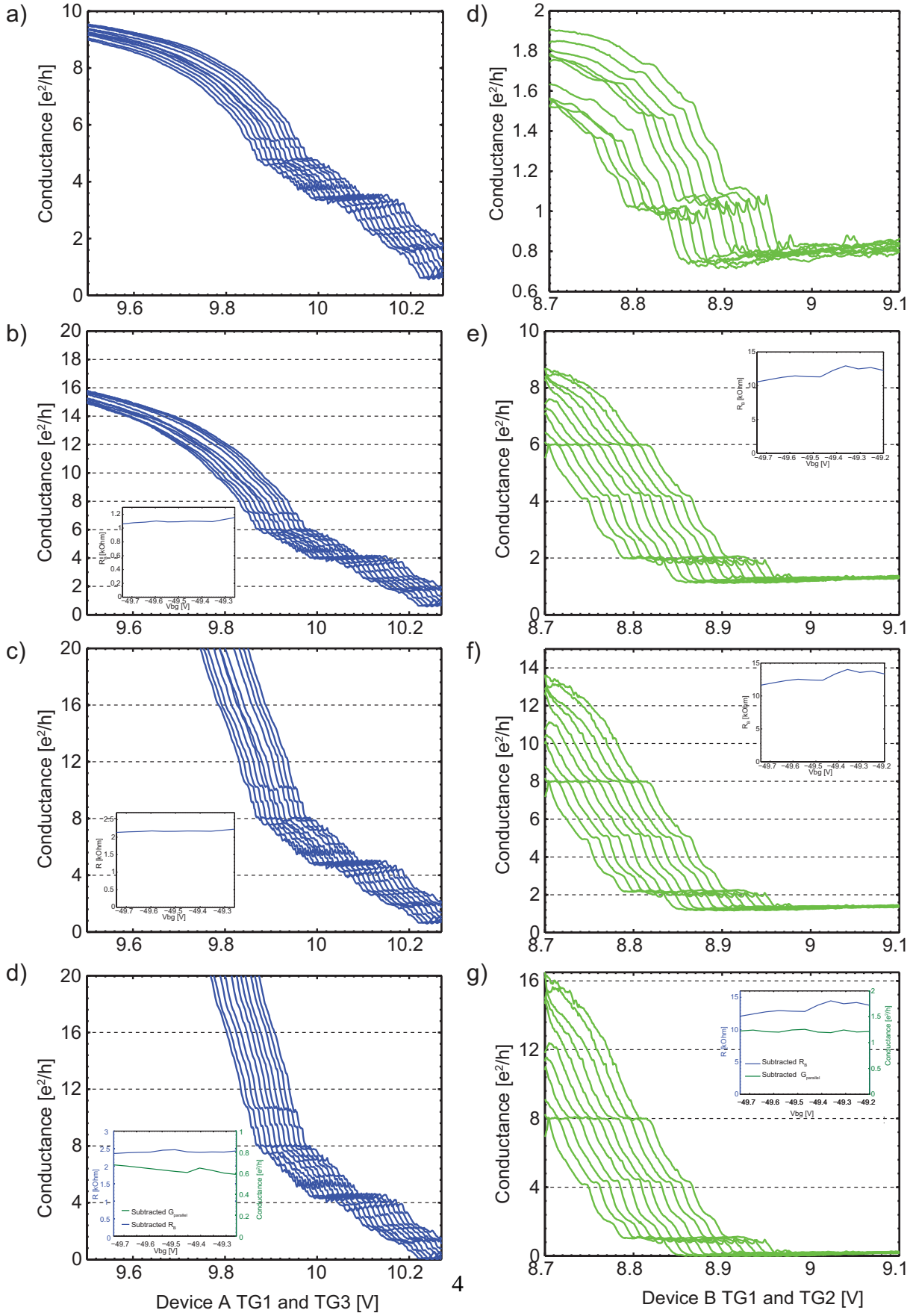
a)
b)
c)
d)
d)
e)
f)
g)
Conductance [e²/h]
Vbg [V]
R [kOhm]
Subtracted G_parallel
Subtracted R_B
Conductance [e²/h]
Device A TG1 and TG3 [V]
Device B TG1 and TG2 [V]

Figure 2