In Situ Reduction of Charge Noise in GaAs/Al$_x$Ga$_{1-x}$As Schottky-Gated Devices

Christo Buizert,[1,2] Frank H. L. Koppens,[1] Michel Pioro-Ladrière,[2] Hans-Peter Tranitz,[3] Ivo T. Vink,[1] Seigo Tarucha,[2,4]
Werner Wegscheider,[3] and Lieven M. K. Vandersypen[1,*]

[1]*Kavli Institute of NanoScience, Delft University of Technology, PO Box 5046, 2600 GA, The Netherlands*
[2]*Quantum Spin Information Project, ICORP, Japan Science and Technology Agency, Atsugi-shi, Kanagawa 243-0198, Japan*
[3]*Institut für Angewandte und Experimentelle Physik, Universität Regensburg, Regensburg, Germany*
[4]*Department of Applied Physics, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, 113-8656, Japan*
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We show that an insulated electrostatic gate can be used to strongly suppress ubiquitous background charge noise in Schottky-gated GaAs/AlGaAs devices. Via a 2D self-consistent simulation of the conduction band profile we show that this observation can be explained by reduced leakage of electrons from the Schottky gates into the semiconductor through the Schottky barrier, consistent with the effect of "bias cooling." Upon noise reduction, the noise power spectrum generally changes from Lorentzian to $1/f$ type. By comparing wafers with different Al content, we exclude that *DX* centers play a dominant role in the charge noise.

The GaAs/AlGaAs two-dimensional electron gas (2DEG) has been of unparalleled importance in the field of mesoscopic physics [1] and has found wide commercial application in high electron mobility transistors (HEMTs) [2]. Today, its unique electronic properties facilitate a variety of important developments, such as spin based quantum information devices [3], Kondo physics [4], electron interferometers [5] and counting statistics [6]. In these, and similar experiments, progress is hindered by uncontrolled charge fluctuations in the solid state environment.

Charge noise has been studied both locally by monitoring conductance fluctuations in a quantum point contact (QPC) or quantum dot [7–16], and on a macroscopic scale using resistance fluctuations in Hall bar structures [16–18]. Several charge switching sites have been proposed, either near the 2DEG [9–11] or in the remote impurity layer [8,16,17] and more specifically the *DX* centers [13]. The charge switching process has been attributed to electron hopping between trap and 2DEG [9–11], electrons leaking from the split gates through the Schottky barrier [12,15] or (thermally activated) switching between different sites or configurations within the impurity layer [8,13,16,17]. Trapping of 2DEG carriers can be excluded as the dominant mechanism since 2DEG density fluctuations are too small [16,17]. Switching in the impurity layer is successful in explaining the complex gating behavior observed in submicron Hall devices by Li *et al.* [17], whereas gate leakage can explain the stabilizing effect of "bias cooling" on Schottky-gated devices [15].

Here we present measurements of conductance fluctuations of a QPC with an additional insulated electrostatic top gate that allows us to tune background charge switching *in situ*. The technique has proven successful in reducing charge noise in nine different devices fabricated in three runs on two separate wafers in both Tokyo and Delft, and we believe it to hold universally for GaAs/Al$_x$Ga$_{1-x}$As

split-gate devices [19]. Furthermore, we examine the mechanism behind this noise reduction, its effect on the noise spectrum, and the nature of the charge traps involved in the switching noise.

A typical device [see Fig. 1(a) inset] has split Schottky gates (20 nm Ti/Au) deposited on a GaAs/AlGaAs heter-
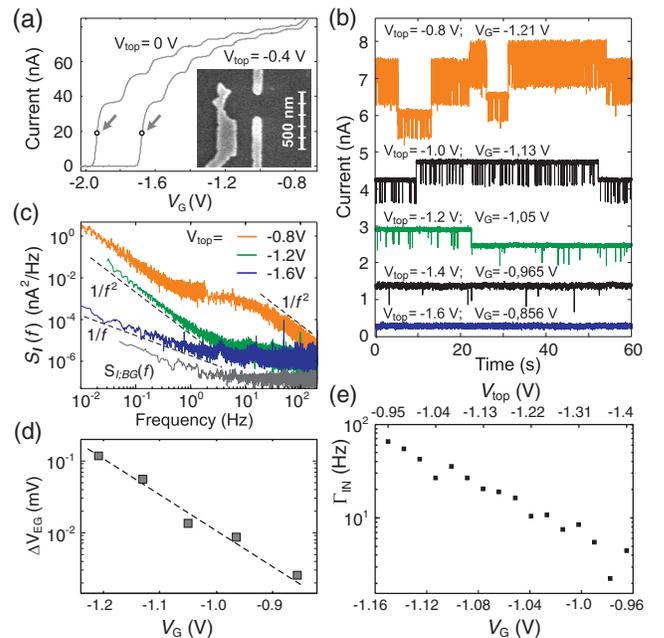

FIG. 1 (color online). (a) QPC pinch-off traces (two terminal, $V_{SD} = 0.8$ mV, $T = 40$ mK). The operating point is marked. Wafer DLF1, see Table I. Inset: a Scanning Electron Micrograph of a typical device layout before deposition of the insulated top gate. (b) QPC time traces for indicated gate voltages, offset for clarity. (c) Power spectra $S_I(f)$ from FFT of time traces; setup noise background $S_{I;BG}(f)$ recorded at zero V_{SD}. (d) Equivalent gate voltage noise ΔV_{EG}. (e) Measured trapping rate Γ_{in} extracted from time traces as in (b), but for a different QPC.

ostructure with a 2DEG 90 nm below the surface. These gates are covered by a 100 nm thick *e*-beam defined negative resist calixarene layer, which serves as an electrical insulator [20,21]. Finally, we deposit a 400 nm thick Ti/Au top gate with dimensions much larger than the Schottky gates. By applying a voltage V_G to two Schottky gates that approach each other, we deplete the 2DEG underneath and form a QPC. Typical QPC pinch-off traces with quantized conductance steps are shown in Fig. 1(a), for two values of the voltage applied to the insulated top gate, V_{top}.

We operate the QPC halfway the first plateau ($G_{QPC} \approx e^2/h$) where the slope dI_{QPC}/dV_G is steepest and the signal is most sensitive to changes in the electrostatics. When charge traps close to the QPC are filled or emptied the QPC conductance is modified. The QPC thus provides a local probe of the charge noise.

Figure 1(b) illustrates that biasing the top gate can have a pronounced effect on the charge noise. The topmost trace is very noisy, with several readily identified two-level fluctuators (from their amplitude, we estimate the charge traps to lie within a few 100 nm from the QPC channel). In the traces below it, V_{top} was made more negative in -0.2 V increments. Simultaneously, the voltage V_G on the Schottky gates was made more positive to maintain $G_{QPC} \approx e^2/h$. We see that the fluctuators are eliminated one by one when V_{top} (V_G) is made more negative (positive).

Figure 1(c) shows corresponding power spectral densities $S_I(f)$ obtained by fast Fourier transform (FFT). The power spectrum $S_I(f)$ of two-level random telegraph noise (RTN) is a Lorentzian which is flat at low frequencies and falls off as $1/f^2$ above the corner frequency $\tau_{eff}^{-1} = \tau_u^{-1} + \tau_d^{-1}$, where τ_u (τ_d) is the average time spent in the low (high) current state [22]. For the initial many-level RTN [topmost trace in Fig. 1(b)], $S_I(f)$ contains Lorentzian contributions with different corner frequencies [topmost trace in Fig. 1(c)]. Once the RTN is eliminated through V_{top} the remaining noise has a $1/f$ power spectrum over a wide frequency range, indicative of an ensemble of fluctuators with a homogeneous distribution of time scales τ_{eff} [22]. Also for devices that did not exhibit pronounced RTN at $V_{top} = 0$ the overall noise level was strongly reduced when

TABLE I.   Heterostructure wafer properties.

Name	x	Donor depth (nm)	n (cm^{-2})	μ (cm^2 V^{-1} s^{-1})
DLF1[a]	0.27	0–70	4.5×10^{11}	
TOK1[a]	0.27	5–65	3.0×10^{11}	1.5×10^6
REG1	0.11	0–70	1.8×10^{11}	8.5×10^5
REG2	0.2	0–70	3.2×10^{11}	2.0×10^6
REG3	0.3	0–70	2.8×10^{11}	1.4×10^6
REG4	0.1	50	2.1×10^{11}	2.1×10^6
REG5	0.2	50	2.3×10^{11}	2.0×10^6
REG6	0.3	50	1.3×10^{11}	9.7×10^5

[a]purchased from Sumitomo Electric Industries Ltd., Japan.

a negative V_{top} was applied and the QPC was operated at less negative V_G.

We quantify the noise level in units of equivalent gate voltage noise ΔV_{EG}, i.e., the voltage noise level applied to the the Schottky gates that would produce the same conductance fluctuations as caused by the charge noise processes. As in Ref. [14] we use the integrated spectral density over a finite frequency range:

$$\Delta V_{EG} = \sqrt{2 \int_{0.1}^{100} [S_I(f) - S_{I;BG}(f)] df} \Big/ \left(\frac{dI_{QPC}}{dV_G} \right). \quad (1)$$

We scale by dI_{QPC}/dV_G to account for device sensitivity. Setup noise $S_{I;BG}(f)$ [see Fig. 1(c)] is subtracted. We also verified that $S_I(f) \propto V_{SD}^2$, as expected for QPC conductance fluctuations. Figure 1(d) shows that ΔV_{EG} is reduced exponentially with less negative V_G.

More insight can be obtained from the V_{top} dependence of the RTN time scales. In this case we select a device where a single fluctuator dominates over a relatively large V_G range. V_{top} is stepped from -0.95 to -1.4 V in increments of -30 mV, while simultaneously V_G is stepped from -1.15 to -0.965 V ensuring $G_{QPC} \approx e^2/h$. For each gate voltage setting we record 80 s of the bistable current from which we can derive the trapping and release rates $\Gamma_{in} = \tau_u^{-1}$ and $\Gamma_{out} = \tau_d^{-1}$ of the fluctuator. In this V_{top} range Γ_{in} is reduced by over an order of magnitude as shown in Fig. 1(e). Whereas this trend in Γ_{in} is characteristic of all measured devices, changes in Γ_{out} are generally less pronounced, with both increasing and decreasing trends occurring. Both rates were found to be independent of temperature up to 4.2 K, indicative of tunneling rather than a thermally activated process.

The clear dependence of the RTN on gate voltages, and hence on the conduction band profile below the gates, suggests that its origin is associated with tunnel processes along the growth direction. Specifically, electrons could tunnel from the metal gates through the Schottky barrier to charge traps in the AlGaAs layer (Γ_{in}), and subsequently to the 2DEG (Γ_{out}) [12,15].

We therefore study in detail how the configuration of gate voltages $\{V_G; V_{top}\}$ affects the conduction band profile $U_C(z)$ and the opacity of the Schottky barrier. To obtain realistic $U_C(z)$ profiles a 1D calculation would not suffice as the Schottky gate would fully screen changes in V_{top}. We have performed 2D self-consistent simulations of our device using the nextnano^3 software package [23]. The simulated structure consists of a cross-section of the stacked layers with the Schottky gate embedded in the calixarene insulating layer [Fig. 2(a)].

Here we compare two configurations; the first uses only the Schottky gate to deplete the 2DEG ($V_G = -1.0$ V, $V_{top} = 0$ V), whereas the other utilizes both gates ($V_G = -0.6$ V, $V_{top} = -1.7$ V). These values give identical carrier depletion width (along x) at the 2DEG. The corresponding conduction band profiles, $U_C(z)$, directly below
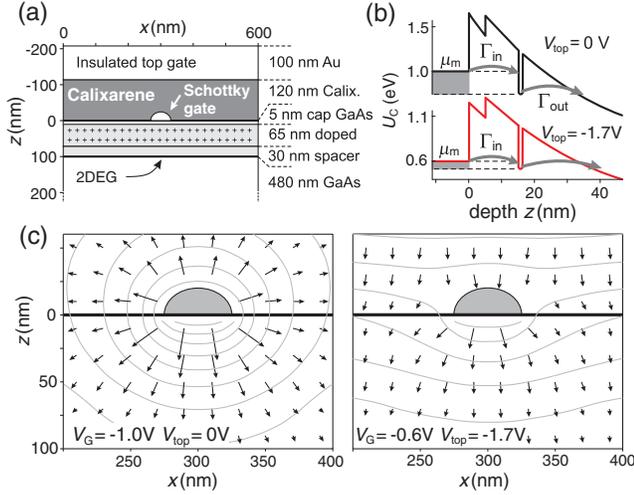
FIG. 2 (color online). (a) Simulated 2D device structure with $Al_{0.26}Ga_{0.74}As$ doped- and spacer layer. Si doping $n_{Si} = 0.3 \times 10^{18}$ cm^{-3}; Calixarene simulated as SiO_2 with $\varepsilon_r = 7.1$. (b) Simulated $U_C(z)$ under the Schottky gate at $x = 300$ nm. Tunneling into a localized trap with fixed energy below U_C occurs most easily from the quasi-Fermi level in the metal lead (μ_m) where the barrier is lowest (this is generally an inelastic process). (c) Quiver plot of the simulated electric field and equipotential lines near the Schottky gate (gray shaded) for the indicated voltage configurations.

the Schottky gate are shown in Fig. 2(b). We added a possible deep trapping state in the illustration; many such states have been identified in doped AlGaAs quantum well structures [24]. Clearly the position and energy of the trap influence Γ_{in} and Γ_{out}. However, for any given trap, the Schottky barrier is higher for more negative V_{top} (positive V_G). Even though at the surface $U_C(0)$ is always ≈ 0.7 eV above μ_m due to surface states, the slope $\partial U_C/\partial z$ is less steep in the lowermost configuration, and the overall barrier is higher. Furthermore by making V_{top} more negative the trap energy is lifted relative to μ_m, reducing the number of allowed initial orbitals (in gray). Eventually leakage is eliminated when the trap energy is lifted above μ_m. In summary, partial depletion using the insulated top gate reduces or even eliminates tunneling from the Schottky gate.

Figure 2(c) shows the 2D electrostatics for both configurations. Note that the radial field in the left configuration also allows tunneling in more sideways directions (possibly also to traps at the surface) and that Γ_{out} depends on the electric field at the location where the electron is trapped. This can lead to a wide range of behaviors for the influence of V_{top} on Γ_{out}, as observed.

This interpretation is entirely consistent with the reduction of charge noise due to "bias cooling" (BC); see Fig. 3 and [15]. BC is a technique where a device is cooled down with a positive bias V_{BC} applied to the Schottky gates, so that carriers are frozen in at low temperature in deep traps, known as DX centers [25]. When V_{BC} is subsequently removed, this (nonequilibrium) trap occupation can be

maintained indefinitely. The presence of these additional negative charges lowers V_G required to deplete the 2DEG, as seen in the insets of Fig. 3, and discussed further below.

We here use this BC technique to examine the nature of the traps involved in switching noise. We focus thereby on the question whether DX centers play an important role in charge noise, as is often claimed. For this purpose, we have fabricated split-gate QPCs on six different modulation-doped $GaAs/Al_xGa_{1-x}As$ 2DEG heterostructure wafers, where the Al mole fraction x ranged from 0.1 to 0.3 (the dopants were included either uniformly or in a monatomic delta layer, see REG1-6 in Table I). For $x = 0.1$ the trapping energy of DX centers lies on the order of 0.1 eV above the conduction band edge U_C [26], so the DX centers are incapable of trapping electrons (indeed BC does not shift the operation point V_G, see Fig. 3 inset). For $x = 0.2$ and $x = 0.3$ the DX levels lie around and well below U_C respectively, so they can trap charges during cooldown (additional energy is needed to escape once trapped [26]). Thus, for $x = 0.2$–0.3, DX centers could potentially act as the intermediate traps responsible for charge noise; for $x = 0.1$, they cannot.

Of each wafer a chip with two QPCs was repeatedly cooled down to 4.2 K, each time with different V_{BC}. For both QPC's, time traces were recorded with the respective V_G set such that $G_{QPC} \approx e^2/h$. Figure 3 shows the measured equivalent voltage noise level ΔV_{EG}, as calculated
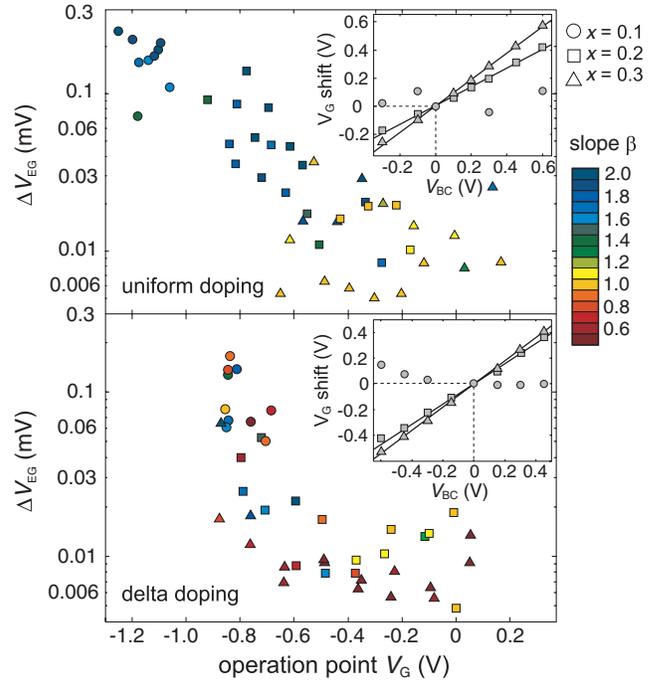

FIG. 3 (color). Effect of BC on charge noise for uniform doping (REG1-3, upper panel) and delta doping (REG4-6, lower panel). Noise levels calculated using Eq. (1), the color of the data points codes for the local spectral slope $S_I(f) \propto f^{-\beta}$. The insets show the observed shift in operation voltage V_G, at given V_{BC}. Each point is averaged over two devices. $T = 4.2$ K.

with Eq. (1) for $f = 1, \ldots, 35$ Hz, where each data point corresponds to a single cooldown of a device. The color of the data points codes for the local spectral slope $\beta(f) = -\partial \ln S_I(f)/\partial \ln f$ around $f = 10$ Hz.

A clear pattern emerges, despite the large differences in heterostructure composition and the random location of switching sites upon thermal cycling. For very negative V_G we observe high noise levels, often with predominantly Lorentzian spectra ($\beta = 2$, blue dot), i.e., the signal is dominated by a few active charge traps in the vicinity of the QPC. Via BC we can operate the device at lower V_G, leading to systematically reduced noise levels, similar to the case when using V_{top}. Around $V_G \sim -0.4$ V the noise level could not be lowered further. Again, the remaining noise is predominantly of the $1/f$-type (yellow dots), and originates from charge noise in the sample. Other noise contributions, such as instrumentation (substracted), V_G noise (<1 μV peak to peak) and shot noise were all at least an order of magnitude smaller. The delta-doped wafers often showed $\beta < 1$ (red dots), indicating a nonuniform distribution of corner frequencies.

Comparing the results for heterostructures REG1-6, we observe that the heterostructures with $x = 0.1$ in fact show the highest ΔV_{EG}. Those with $x = 0.3$ exhibit the least charge noise. Furthermore all heterostructures share the common trend of lower ΔV_{EG} with less negative V_G, despite the differences in Al fraction. Based on these observations we exclude the DX center as the dominant trapping site for leaking electrons. Also the suggestion that DX charge state bistability causes the RTN [13] is refuted. The low band gap energy of $Al_{0.1}Ga_{0.9}As$ does however make the Schottky barrier more transparent, which might explain why REG4 is much more noisy than REG5,6 for the same V_G.

Altogether, we consistently observe that less negative V_G improves charge stability. This can be achieved either by a negative V_{top}, via BC, or a combination of both. Despite the similarity between the two approaches for noise reduction, it is clear that the resulting electric field profiles are very different, so noise levels and time characteristics may differ even for the same V_G. We note that V_{BC} is limited to about $+600$ mV, which was sometimes not sufficient to stabilize a device, while good stability was achieved with sufficiently negative V_{top}. The insulated gate approach is thus not only more flexible but proved more powerful as well.

We conclude from our measurements that charge noise in gated GaAs/AlGaAs devices is dominated by trapping of electrons leaking in from the Schottky gates. After this tunneling mechanism is reduced or eliminated, a baseline charge noise remains, that is presumably of a different origin. This insight allows us make use of heterostructures that would otherwise suffer from excessive charge noise. It also points to a way of reliably obtaining heterostructure devices with little charge noise, for instance by introducing an additional high bandgap AlAs layer beneath the cap layer, or a thin insulating layer underneath the Schottky gates.

*L.M.K.vandersypen@tudelft.nl

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